**University of engineering & technology Peshawar**



**Circuit & system-1**

**Lab report # 6**

**Fall 2020**

**Submitted by: Ashfaq Ahmad**

**Section: B**

**Reg No: 19PWCSE1795**

**Semester: 2nd**

**Submitted to:**

**Eng: FAIZ ULLAH**

**Department Of Computer System Engineering**

**ASSESSMENT RUBRICS LAB # 6**

**Verification of KCL using PSPICE**

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| --- | --- | --- | --- | --- |
| **LAB REPORT ASSESSMENT** | | | | |
| **Criteria** | **Excellent** | **Average** | **Nill** | **Marks Obtained** |
| 1. **Objectives of Lab** | All objectives of lab are properly covered  [Marks 0.5] | Objectives of lab are partially covered  [Marks 0.25] | Objectives of lab are not shown  [Marks 0] |  |
| 1. **Kirchhoff’s Current Law**   **(Statement, Mathematical Expression, Circuit Diagram)** | Correct KCL statement and mathematical expression is written. Circuit diagram shown is correct and properly labeled  [Marks 1] | KCL statement or mathematical expression or circuit diagram is missing or circuit diagram is not properly labeled  [Marks 0.5] | |  |
| 1. **PSPICE**   **Simulator** | Brief introduction of PSPICE simulator  [Marks 1] | Brief introduction of PSPICE simulator  Is not shown  [Marks 0] | |  |
| 1. **Procedure** | All experimental steps are shown in detail  [Marks 1.5] | Some of the experimental steps are missing [Marks 1] | Experimental steps are missing  [Marks 0] |  |
| 1. **Observations & Calculations** | All experimental results are completely shown in form of table for both cases of using same resistors and for different resistors with varying applied source voltage  [Marks 4] | Experimental results are partially shown and some of the observations are missing  [Marks 2] | No experimental results are shown  [Marks 0] |  |
| 1. **Analysis** | Analysis and discussion about all experimental results are shown  [Marks 2] | Analysis and discussion about experimental results are partially shown  [Marks 1] | Analysis is not shown  [Marks 0] |  |
| Total Marks Obtained:\_\_\_\_\_\_\_\_\_\_                                                              Instructor Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | | | |

1. **Objectives:**

* To know about KCL law.
* To understand how we verify KCL law by using PSPICE.
* To learn KCL mathematical expression and circuit diagram.
* To know PSPICE software.

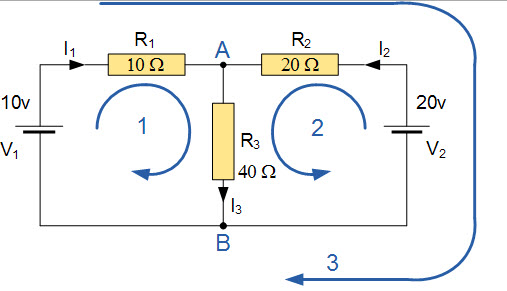
1. **Kerchief’s current law (KCL):**

* Kirchhoff's Current **Law** (**KCL**) is Kirchhoff's first **law** that deals with the conservation of charge entering and leaving a junction.

**Statement:**

* Kerchief current law states that for a parallel path the total current entering a circuits junction is exactly equal to the total current leaving the same junction.
* In other we can say that The algebraic sum of all currents entering and exiting a node must equal zero.

**Circuit diagram:**



**Mathematical expression:**

Mathematical expressions for above circuit are,

I1+I2+ (-I3) =0

General expression is,

I1+I2+I3…………IN=0

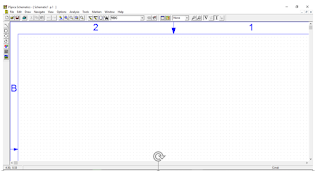
**NOTE:** The current entering the junction will be taken as +ive, while the leaving one will be taken as –ive and vice versa...

1. **PSPICE simulator:**

PSPICE is a SPICE analog circuit and digital logic simulation program for Microsoft Windows. The name is an acronym for Personal SPICE - SPICE itself being an acronym for Simulation Program with Integrated Circuit Emphasis. PSPICE is a circuit analysis tool that allows the user to simulate a circuit and extract key voltages and currents. Information is entered into PSPICE via one of two methods; they are a typed 'Net List' or by designing a visual a schematic which is transformed into a net list.

1. **Procedure:**

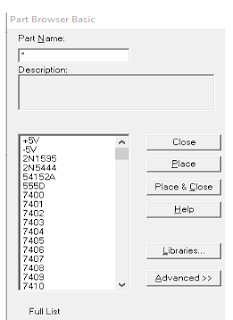
* Open up PSPICE schematics.

[](https://4.bp.blogspot.com/-IJc2Mc3Dbsg/WSbDwyYlN5I/AAAAAAAAAw8/nUYf_aeXyhc4mXTyMTSwpE4JFEvpI-3KwCEw/s1600/3.PNG)

* Click on get new part.

[](https://2.bp.blogspot.com/-3m4LbLuSglk/WSbDwhjWqBI/AAAAAAAAAw4/4_L3vD1lkg4GnfnFrOOiXbITWOdT0cXJgCEw/s1600/4.PNG)

* Then place the option which you want to have.

**[](https://3.bp.blogspot.com/-heJzU4_tn3U/WSbDwyA8l8I/AAAAAAAAAxA/mIHM_w2i-JEWooeck8QQmmhNh3H3kCeowCEw/s1600/5.PNG)**

Here we need three resistors, DC voltage source and ground link.

* After selecting the things and options we want, press on simulate.

|  |
| --- |
| <https://2.bp.blogspot.com/-TMNdVJ5kZME/WSbDxGsTK2I/AAAAAAAAAxE/lItTk-JwHEMvbTULfAIR9c0E-4ljO25_QCEw/s1600/6.PNG> |

* Then after pressing simulate, press V and I mentioned in the menu bar to show the voltage drop and current.

[](https://4.bp.blogspot.com/-rTBldk9pz6Q/WSbDxFjMqkI/AAAAAAAAAxI/Rx1XmdYKHZcH4ERbuj_yMz7NI7QUZ2CsQCEw/s1600/7.PNG)

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| --- |
| **Circuit diagrams for same resisters,**  [https://2.bp.blogspot.com/-NZkp_bFmR-w/WSbDxeNTyDI/AAAAAAAAAxU/l54TSw5dLQQ0NgRls_KdUYy7lQFO3ulwwCEw/s320/8.PNG](https://2.bp.blogspot.com/-NZkp_bFmR-w/WSbDxeNTyDI/AAAAAAAAAxU/l54TSw5dLQQ0NgRls_KdUYy7lQFO3ulwwCEw/s1600/8.PNG)[https://3.bp.blogspot.com/-25Fho6Yc2PY/WSbDwHy230I/AAAAAAAAAxU/9izVj3IOcEMeOBxKXSdHU_DaJ7G79ee_QCEw/s320/10.PNG](https://3.bp.blogspot.com/-25Fho6Yc2PY/WSbDwHy230I/AAAAAAAAAxU/9izVj3IOcEMeOBxKXSdHU_DaJ7G79ee_QCEw/s1600/10.PNG) |

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| --- |
| Circuit diagram for different resisters.  [https://4.bp.blogspot.com/-Cku2bsPfdGM/WSbDxg8UuVI/AAAAAAAAAxU/W1qfiGVJCBg4s9sFRFWZSXzTjFlzei31gCEw/s320/9.PNG](https://4.bp.blogspot.com/-Cku2bsPfdGM/WSbDxg8UuVI/AAAAAAAAAxU/W1qfiGVJCBg4s9sFRFWZSXzTjFlzei31gCEw/s1600/9.PNG) |

1. **Observation and calculation**

Data table for same resisters and varying voltages:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S no** | **vs** | **R1** | **R2** | **R3** | **I1** | **I2** | **I3** | **1I=I2+I3** |
| **1** | 5 | 1k | 1k | 1k | 3.333A | 1.667A | 1.667A | 1.667+1.667 = 3.33A |
| **2** | 8 | 2730 | 2730 | 2730 | 1.22mA | 610.5u | 610.5u | 610.5u+610.5u = 1.22mA |
| **3** | 10 | 100 | 100 | 100 | 5A | 2.50A | 2.50A | 2.50+2.50= 5A |
| **4** | 15 | 10 | 10 | 10 | 3mA | 1.5mA | 1.5mA | 1.5m+1.5m= 3mA |
| **5** | 20 | 200 | 200 | 200 | 8A | 4A | 4A | 4+4= 8A |

Data table for different resisters and varying voltages:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S NO** | **VS** | **R1** | **R2** | **R3** | **I1** | **I2** | **I3** | **1I=I2+I3** |
| **1** | 5 | 2.73k | 2k | 1.5k | 1.39mA | 597.3uA | 795.5uA | 795.5+597.3 =1.39mA |
| **2** | 8 | 1K | 10 | 300 | 10.55A | 7. 55A | 3A | 7.55+3= 10.55 |
| **3** | 10 | 700 | 35 | 60 | 6.33mA | 4.22mA | 2.11mA | 4.22m+ 2.11m= 6.33mA |
| **4** | 15 | 150 | 200 | 300 | 4A | 2.36A | 1.64A | 2.36A+1.64A= 4A |
| **5** | 20 | 100 | 200 | 1K | 3mA | 2.3mA | 0.7mA | 2.3m+0.7m= 3mA |

1. **Analysis:**

According Kirchhoff’s Current Law, if the currents entering the junction are taken as positive, while the ones leaving the junction are taken as negative, its algebraic sum will be equal to zero, thus from above data we proved that I1 + I2 +(- I3 )= 0

So we can confirm by analysis that Kirchhoff’s current law (KCL) which states that “the algebraic sum of the currents at a junction point in a circuit network is always zero” is true and correct.

The end